REMARKS

Claims 1-95 are pending in the present application. The Examiner has objected to the drawings and has rejected claims 1-95.

I. OBJECTION TO THE DRAWINGS

The Examiner objected to the drawings as being informal. Applicants respectfully submit herewith a formal set of drawings. It is therefore respectfully requested that the objection be withdrawn with respect to the drawings.

II. REJECTION OF CLAIMS 1-18, 20-38, 40-59 AND 61-94 UNDER 35 U.S.C. § 102(e)

Claims 1-18, 20-38, 40-59 and 61-94 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,194,962 B1 ("Chen"). Applicants respectfully traverse the rejection.

A. Claims 1-18, 20 and 21

Chen does not describe each and every element as set forth in claim 1. For example, claim 1 recites "a plurality of differential pairs coupled together through a common differential output". On the other hand, Chen describes a first differential pair MN1/MN2 and a second differential pair MP1/MP2 that are not coupled via a common differential output. For example, in FIG. 3, none of the differential outputs (e.g., the drains) of the first differential pair MN1/MN2 are coupled to any of the differential outputs (e.g., the drains) of the second differential pair MP1/MP2 via a common differential output. For at least the above reasons, Chen does not anticipate claim 1 and its dependent claims (i.e., claims 2-18, 20 and 21).

Furthermore, Chen does not describe each and every element as set forth in claims 2-18, 20 and 21. For example, claim 6 recites that "the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form the differential output". As is clear from FIGS. 3 and 4 of Chen, the drain of transistor MN1 is not coupled to the drain of transistor MP1 or transistor MP2, and the drain of transistor MN2 is not coupled to the drain of transistor MP1 or transistor MP2. Furthermore, the drain of transistor MP1 is not coupled to the drain of transistor MN1 or transistor MN2, and the drain of transistor MP2 is not coupled to the

drain of transistor MN1 or transistor MN2. Thus, Chen does not anticipate claim 6. In another example, claim 12 recites that "the bias circuit generates a bias current which is substantially independent of temperature". The Examiner maintains that col. 3, line 47 to col. 4, line 19 of Chen describes these elements. However, the cited text does not even mention temperature and certainly does not describe a bias current which is substantially independent of temperature. Thus, Chen does not anticipate claim 12. In yet another example, claim 13 recites that "the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input". The Examiner maintains that col. 4, lines 3-67; col. 5, lines 3-45 and col. 7, lines 23-67 describe these elements. However, the cited text is silent as to, for example, a first bias current exhibiting a positive temperature coefficient and a second bias current exhibiting a negative temperature coefficient. Thus, Chen does not anticipate claim 13.

It is therefore respectfully requested that the rejection under 35 U.S.C. § 102(e) be withdrawn with respect to claims 1-18, 20 and 21.

B. Claims 22-38, 40 and 41

Chen does not describe each and every element as set forth in claim 22. For example, claim 1 recites "a plurality of amplifying stages each having first and second transistors, the first and second transistors each having first, second and third nodes, the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output". On the other hand, Chen describes a first differential pair MN1/MN2 and a second differential pair MP1/MP2 in which no nodes of the transistor MN1 are coupled to any of the nodes of transistor MP1 or transistor MP2 to form a differential output. Furthermore, no nodes of the transistor MN2 are coupled to any of the nodes of transistor MP1 or transistor MP2 to form a differential output. For at least the above reasons, Chen does not anticipate claim 22 and its dependent claims (i.e., claims 23-38, 40 and 41).

Furthermore, Chen does not describe each and every element as set forth in claims 23-38, 40 and 41. For example, claim 26 recites that "the first nodes each comprises a drain". Since Chen does not describe first nodes as set forth in claim 22, Chen does not describe first nodes, each comprising a drain. Thus, Chen does not anticipate claim 26. In another example, claim 32

recites that "the bias circuit generates a bias current which is substantially independent of temperature". The Examiner maintains that col. 3, line 47 to col. 4, line 19 of Chen describes these elements. However, the cited text does not even mention temperature and certainly does not describe a bias current which is substantially independent of temperature. Thus, Chen does not anticipate claim 32. In yet another example, claim 33 recites that "the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input". The Examiner maintains that col. 4, lines 3-67; col. 5, lines 3-45 and col. 7, lines 23-67 describe these elements. However, the cited text is silent as to, for example, a first bias current exhibiting a positive temperature coefficient and a second bias current exhibiting a negative temperature coefficient. Thus, Chen does not anticipate claim 33.

It is therefore respectfully requested that the rejection under 35 U.S.C. § 102(e) be withdrawn with respect to claims 22-38, 40 and 41.

C. Claims 42-59, 61 and 62

Chen does not describe each and every element as set forth in claim 42. For example, claim 42 recites "a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit". Chen describes an op amp with an input stage 28 and an output stage 34. The input stage includes a first differential pair MP1, MP2 and a complementary second differential pair MN1, MN2. See, e.g., FIG. 3; col. 3, lines 38-45; and col. 4, lines 3-10 of Chen. Thus, Chen describes two stages of an op amp. However, neither the input stage 28 nor the output stage 34 can be switched in or out of the circuit as set forth by claim 42. For example, a "switching/current sense" circuit 32 merely provides a bias current needed to make transistors MN1/MN2 active. See col. 3, lines 60-62 of Chen. However, the circuit 32 does not selectively switch the input stage 28 in or out of the circuit. In fact, the input stage 28 is always in the circuit whether or not the circuit 32 provides a bias current to transistors MN1/MN2. See, e.g., Abstract of Chen ("[s]witching circuitry insures that only one differential pair is active at a time, except in a transition region in which both pairs are partially conducting"). Since the input stage 28 is always active and cannot be switched in or out of the circuit, the output stage 34 receives a signal from the input stage 28,

thereby causing the output stage 34 to also be active. Thus, the output stage 34 cannot be selectively switched in or out of the circuit. For at least the above reasons, Chen does not anticipate claim 42 and its dependent claims (i.e., claims 43-59, 61 and 62).

Furthermore, Chen does not describe each and every element as set forth in claims 43-59, 61 and 62. Since claims 43-59, 61 and 62 recite many of the same or similar elements as recited in claims 23-38, 40 and 41 and since the Examiner used the same or similar arguments in rejecting claims 43-59, 61 and 62 as were used in rejecting claims 23-38, 40 and 41, Applicants respectfully make the same or similar arguments with respect to claims 43-59, 61 and 62 as were made with respect to claims 23-38, 40 and 41. For at least the above reasons, Chen does not anticipate claims 43-59, 61 and 62.

It is therefore respectfully requested that the rejection under 35 U.S.C. § 102(e) be withdrawn with respect to claims 42-59, 61 and 62.

D. Claims 63-79

Chen does not describe each and every element as set forth in claim 63. For example, claim 63 recites "a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level". The Examiner maintains that these elements are illustrated in FIGS. 3 and 4 and described in col. 2, lines 41-61; col. 3, lines 38-57; and col. 5, lines 3-32 of Chen. Applicants have carefully reviewed the cited portions of Chen and cannot find support for a digitally programmable power level and a matching circuit and, in particular, a matching circuit that is substantially independent of the programmed power level. For at least the above reasons, Chen does not anticipate claim 63 and its dependent claims (i.e., claims 64-79).

Furthermore, Chen does not describe each and every element as set forth in claims 64-79. Since claims 64-79 recite many of the same or similar elements as recited in claims 23-38, 40 and 41 and since the Examiner used the same or similar arguments in rejecting claims 64-79 as were used in rejecting claims 23-38, 40 and 41, Applicants respectfully make the same or similar arguments with respect to claims 64-79 as were made with respect to claims 23-38, 40 and 41. For at least the above reasons, Chen does not anticipate claims 64-79.

It is therefore respectfully requested that the rejection under 35 U.S.C. § 102(e) be withdrawn with respect to claims 63-79.

E. Claims 80-94

Chen does not describe each and every element as set forth in claim 80. For example, claim 80 recites "switching means for switching one of the amplifying stages in or out of the amplifier to program power of the amplifier". Chen describes an op amp with an input stage 28 and an output stage 34. The input stage includes a first differential pair MP1, MP2 and a complementary second differential pair MN1, MN2. See, e.g., FIG. 3; col. 3, lines 38-45; and col. 4, lines 3-10 of Chen. Thus, Chen describes two stages of an op amp. However, neither the input stage 28 nor the output stage 34 can be switched in or out of the circuit as set forth by claim 42. For example, a "switching/current sense" circuit 32 merely provides a bias current needed to make transistors MN1/MN2 active. See col. 3, lines 60-62 of Chen. However, the circuit 32 does not selectively switch the input stage 28 in or out of the circuit. In fact, the input stage 28 is always in the circuit whether or not the circuit 32 provides a bias current to transistors MN1/MN2. See, e.g., Abstract of Chen ("[s]witching circuitry insures that only one differential pair is active at a time, except in a transition region in which both pairs are partially conducting"). Since the input stage 28 is always active and cannot be switched in or out of the circuit, the output stage 34 receives a signal from the input stage 28, thereby causing the output stage 34 to also be active. Thus, the output stage 34 cannot be selectively switched in or out of the circuit. Thus, Chen does not describe at least these elements as set forth in claim 80. Furthermore, claim 80 recites "matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power". Since there is no mention of the load coupled to the output stage 34 of the op amp, Chen does not describe any type of matching with respect to such a load. Instead, Chen is merely concerned with trimming an op amp offset voltage. For at least the above reasons, Chen does not anticipate claim 80 and its dependent claims (i.e., claims 81-94).

Furthermore, Chen does not describe each and every element as set forth in claims 81-94. Since claims 81-94 recite many of the same or similar elements as recited in claims 23-38, 40 and 41 and since the Examiner used the same or similar arguments in rejecting claims 81-94 as were used in rejecting claims 23-38, 40 and 41, Applicants respectfully make the same or similar arguments with respect to claims 81-94 as were made with respect to claims 23-38, 40 and 41. For at least the above reasons, Chen does not anticipate claims 81-94.

It is therefore respectfully requested that the rejection under 35 U.S.C. § 102(e) be withdrawn with respect to claims 80-94.

III. REJECTION OF CLAIMS 19, 39, 60 and 95 UNDER 35 U.S.C. § 103(a)

Claims 19, 39, 60 and 95 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of U.S. Patent No. 6,175,279 B1 ("Ciccarelli"). Applicants respectfully traverse the rejection.

Neither Chen nor Ciccarelli, alone or in combination, teaches or suggests each and every element as set forth in claims 19, 39 and 60. For example, claims 19, 39 and 60 recite that either the common differential output or the differential output "comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together". The Examiner admits that Chen does not teach or suggest at least these elements of claims 19, 39 and 60. See Office Action mailed November 19, 2003, at section 3, pages 16 and 17. On the other hand, the Examiner maintains that Ciccarelli teaches or suggests these elements and offers FIG. 5A as well as supporting text in Ciccarelli as evidence in support of the rejection. Nevertheless, at least these elements are not taught or suggested by Ciccarelli. For example, Ciccarelli does not even teach or suggest a differential output or a common differential output in FIG. 5A and thus does not teach or suggest a first output and a second output. Instead, FIG. 5A shows a single-ended low-noise amplifier, thus teaching away from a differential output or a common differential output. FIG. 5A merely shows only one output, RF OUTPUT, to which only capacitor 1536 is coupled. Since Ciccarelli does not teach or suggest another output, Ciccarelli does not teach or suggest an inductor coupled to another output. For at least the above reasons, the Examiner has failed to demonstrate how the combination of Chen and Ciccarelli teaches or suggests each and every element as set forth in claims 19, 39 and 60.

Furthermore, neither Chen nor Ciccarelli, alone or in combination, teaches or suggests each and every element as set forth in claim 95. For example, claim 95 recites that "the amplifying stages comprises a differential output having first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having

second end coupled to the amplifier output". The Examiner admits that Chen does not teach or suggest at least these elements of claim 95. See Office Action mailed November 19, 2003, at section 3, page 17 ("Claim 95 contains similar limitations addressed in claim 19, 39, 60, and therefore is rejected under a similar rationale"). On the other hand, the Examiner maintains that Ciccarelli teaches or suggests these elements and offers FIG. 5A as well as supporting text in Ciccarelli as evidence in support of the rejection. Nevertheless, at least these elements are not taught or suggested by Ciccarelli. For example, Ciccarelli does not even teach or suggest a differential output in FIG. 5A and thus does not teach or suggest a first output and a second output. Instead, FIG. 5A shows a single-ended low-noise amplifier, thus teaching away from a differential output. FIG. 5A shows only one output, RF OUTPUT, to which only capacitor 1536 is coupled. Since Ciccarelli does not teach or suggest another output, Ciccarelli does not teach or suggest an inductor coupled to another output. For at least the above reasons, the Examiner has failed to demonstrate how the combination of Chen and Ciccarelli teaches or suggests each and every element as set forth in claim 95.

It is therefore respectfully requested that the rejection under 35 U.S.C. § 103(a) be withdrawn with respect to claims 19, 39, 60 and 95.

IV. CONCLUSION

In view of at least the foregoing, it is respectfully submitted that the pending claims 1-95 are in condition for allowance. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the below-listed telephone number.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: January 30, 2004

Respectfully submitted,

Michael T. Cruz

Michael T. Cruz
Reg. No. 44,636

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661-2565
Telephone: (312) 775-8084
Facsimile: (312) 775-8100